1st Phase Class Routine: 46th BCS (Special) Batch 253

Class Title	Contents
Software Engineering & Information System	
SE-01 (Both 281 & 971)	➢ Introduction, Software process. Project management. ➢ Software testing. ➢ software reliability and availability, Quality assurance. Concepts of Software reliability, availability and safety.
SE-02 (Only 971)	➢ Requirements engineering processes. System Models: Context, data, behavioral and object models: agile, waterfall model, prototype, SCRUM, Spiral; ➢ Object oriented design techniques: Model, UML use case, class, Real-time software design. System design with reuse. Critical system design dependability, software maintenance, critical system specification and development Verification and validation.
SE-03 Only (971)	➢ Software cost estimation: COCOMO model Halstead formula, Graph: Cel analysis of complexity measures,
SE -04 Only (281)	➢ Cost impact of Software defects. Function based metrics and bang metrics. Metrics for analysis and design model. Metrics for source code, testing and maintenance ➢ Analysis Concepts and principles: requirement analysis, Analysis modeling, data modeling. Design concepts and principles, Architectural design, User Interface design,
SE-05 (Only 281)	➢ Different types of information, qualities of information. ➢ Designing Objects with responsibilities. GRASP patterns with General Principles in assigning responsibilities: Information expert, Creator, Low Coupling and High Cohesion, Creating design class diagrams and mapping design to codes.
Microprocessor & Interfacing	
MP-01 (Both 281 & 971)	➢ Microprocessor and microcomputers. ➢ Introduction to microprocessor: ➢ overview of computer architecture, ➢ evolution of microprocessors, ➢ difference between microprocessor and microcontroller; ➢ Intel 8086 microprocessor: Internal architecture, register structure, programming model, addressing modes and instruction sets. basic architecture of 8086, memory segmentation, flags, addressing modes, pins & signals, single and multi-processor systems; ➢ Microprocessor programming: instruction sets, introduction to assembly language programming; Tools: assemblers, debuggers, development systems;
MP-02 (Only 281)	➢ Clock and bus controller interfacing: clock generator, bus demultiplexer, bus controller interfacing; ➢ Memory Interfacing: SRAM and EEPROM interfacing, ➢ Types of I/O: parallel I/O, programmed I/O, interrupt driven I/O, I/O port address decoding, programmable peripheral interface (8255A), ➢ interface examples– Keyboard matrix, LCD/7-Segment display, printer, stepper motor, A/D and D/A converter;

MP-03 (Only 281)	➢ Timer interfacing: The 8254 programmable interval timer (PIT), timing applications; ➢ Serial I/O interface: asynchronous and synchronous communication, physical communication standard-EIA RS232, programmable communication interface, interfacing serial I/O devices- mouse, modem, PC Keyboard; ➢ Interrupts: interrupt driven I/O, software & hardware interrupts, interrupt vectors and vector table, interrupt processing, programmable interrupt controller (8259A), DMA: DMA controller (8237).
MP-04 (Only 971)	➢ Evolution of microprocessor. Architecture of a general-purpose microprocessor and its operation. Addressing modes. ➢ Common instruction types: Basic assembly instruction set. ➢ Interrupts its classification and interrupt handling, ➢ Memory management in Intel 80x86 family: Real-mode memory management, segmentation and segmented to physical address translation. Protected mode memory management: Segmentation and virtual addressing, segment selectors and descriptors and tables. ➢ Intel 80386 and 80486 register formats. Paged memory operation and TLB structure I/O port organization and accessing. ➢ Interfacing the keyboard, printer and monitor. Structure and operation of certain chips as 8255A, 8253, 8272, 8259A, 8237. Bus interfaces and micro controllers.
Computer Organization & Architecture	
CA-01 (Only 971)	➢ Information representation; ➢ Measuring performance; ➢ Instructions and data access methods: operations and operands of computer hardware, representing instruction, addressing styles; ➢ Processor design: data paths & single cycle and multicycle implementations; ➢ Pipeline: pipelined Datapath and control, superscalar and dynamic pipelining; Memory organization: cache, virtual memory, channels.
CA-02 (Both 281 & 971)	➢ Arithmetic Logic Unit (ALU) operations, floating point operations, designing ALU; ➢ Control Unit design - hardwired and microprogrammed ➢ Pipeline processors. Hazards; Exceptions; ➢ Exceptions System organization Bus and hazards I/O subsystem and I/O processor
CA-03 (Only 971)	➢ Interrupts systolic arrays and fault-tolerant computers. ➢ Parallel processing: Concept, ➢ Caches Memory organization. ➢ Fundamentals of computer design.
Compiler Design	
CD -01 (Only 971)	➢ Introduction to compiler. Basic issues, lexical analysis, logical analysis, syntax analyses. ➢ Semantic analysis, type checking, run-time environments, code generation, code optimization and language theory.
Theory of Computation	
TOC-01 (Only 281)	➢ Language theory; Finite automata: deterministic finite automata, nondeterministic finite automata,

	➢ Equivalence and conversion of deterministic and nondeterministic finite automata, pushdown automata; ➢ Context free languages; Context free grammars; Turing Machines: basic machines, configuration, computing with Turing machines

Please Call to : 01518668951 if any queries